Agenda

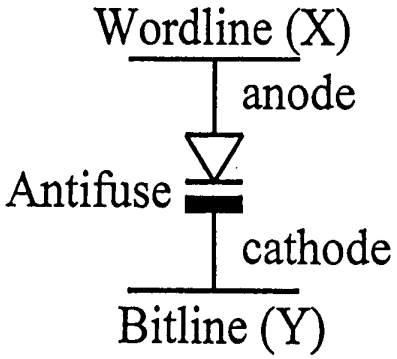
- Memory cell
- Fabrication process
- Device organization
- Write operation
- Read operation
- Bit area comparison
- Summary

Fig. 1

New Sheet

Memory Cell (1/3)

- Two-terminal cell contains a diode and antifuse.
- Wordlines and bitlines are shared between layers.



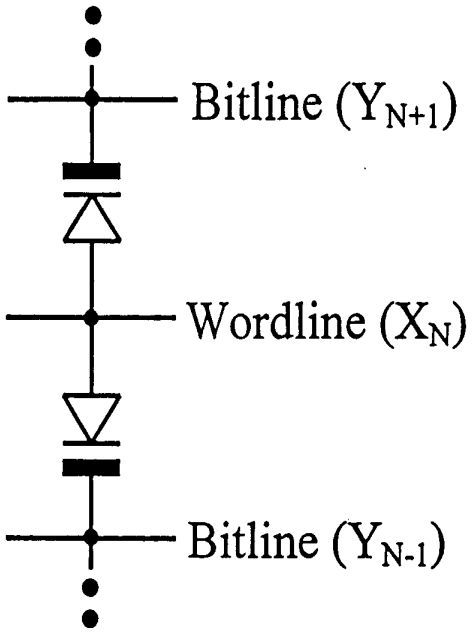


Fig. 2

New Sheet

Memory Cell (2/3)

- Cells built from polycrystalline silicon.
- Stacked for maximum density.

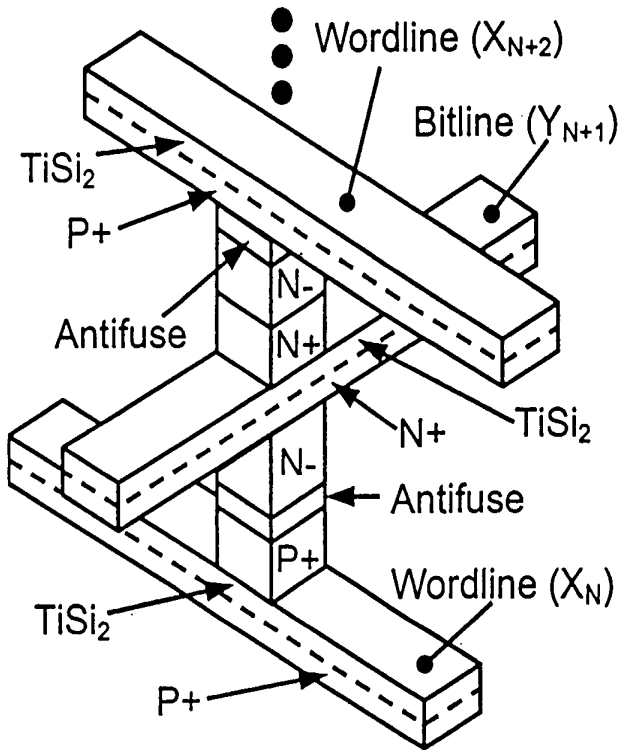


Fig. 3

New Sheet

Memory Cell (3/3)

- Cell states:
  - Unprogrammed "1": initial state of all cells.
  - Programmed "0": Antifuse oxide is ruptured, leaving the diode.
- Antifuse rupture is irreversible.

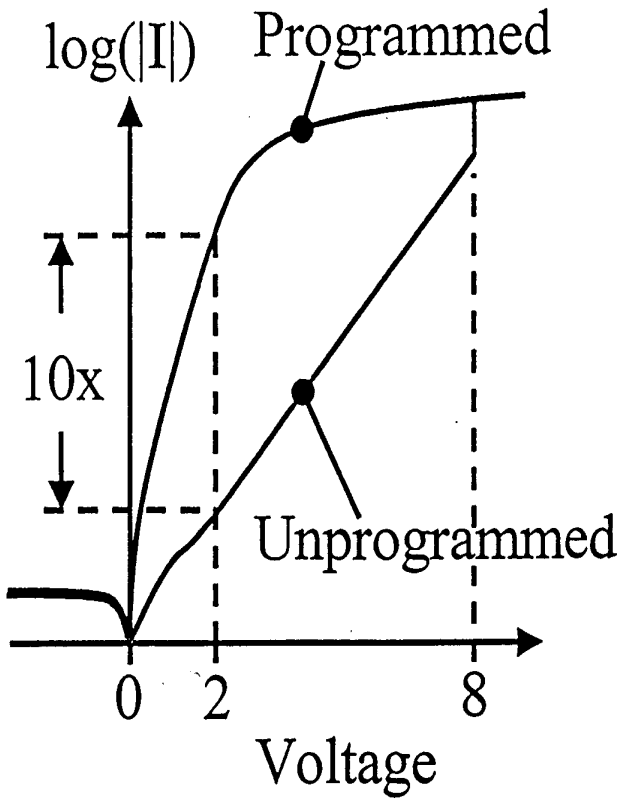


Fig. 4

New Sheet

Process Highlights

- 0.25μm Nwell CMOS:
  - Single 17.5nm gate oxide;
  - 2 tungsten layers ("R1" and "R2") for transistor interconnect.
- 8-high stack of memory cells:
  - 5 wordline layers, 4 bitline layers;
  - Cell is 0.50μm x 0.50μm x (1/8);
  - Vias from array to CMOS.
- 1 Al layer for bond pads, global signals and power distribution.

Fig. 5

New Sheet

Array of Stacked Memory Cells

- Wordlines: X{1, 3, 5, 7, 9}.
- Bitlines: Y{2, 4, 6, 8}.
- (8+1) wiring levels give (8) layers of cells.
- $TiSi_2$ liners reduce sheet rho (2-3 Ω/□).

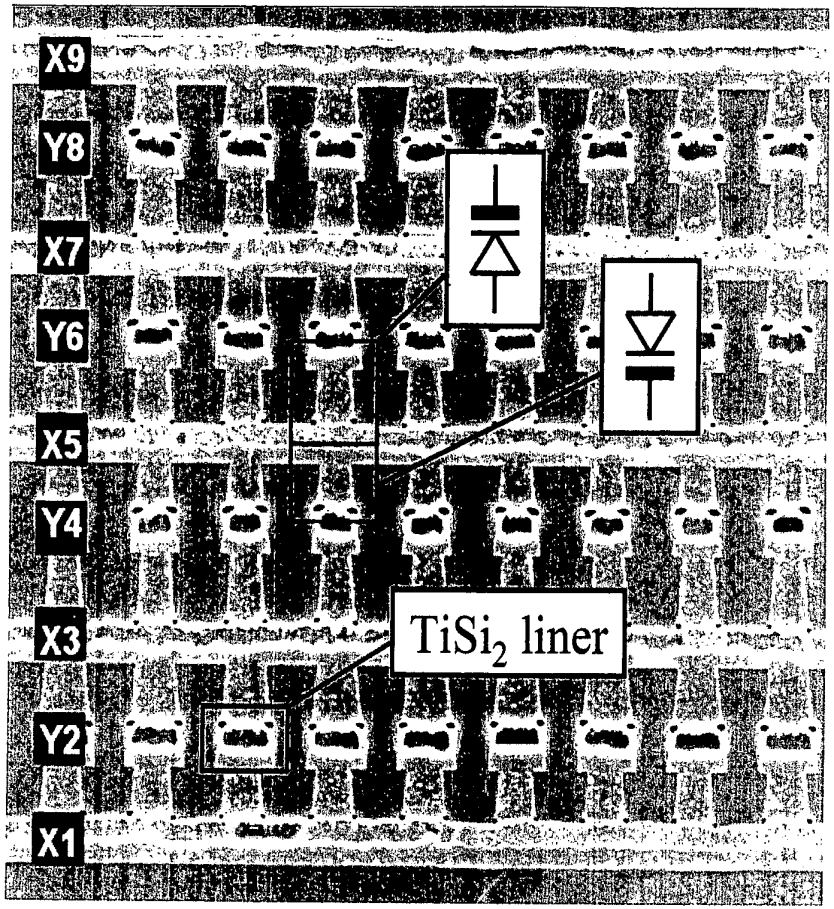
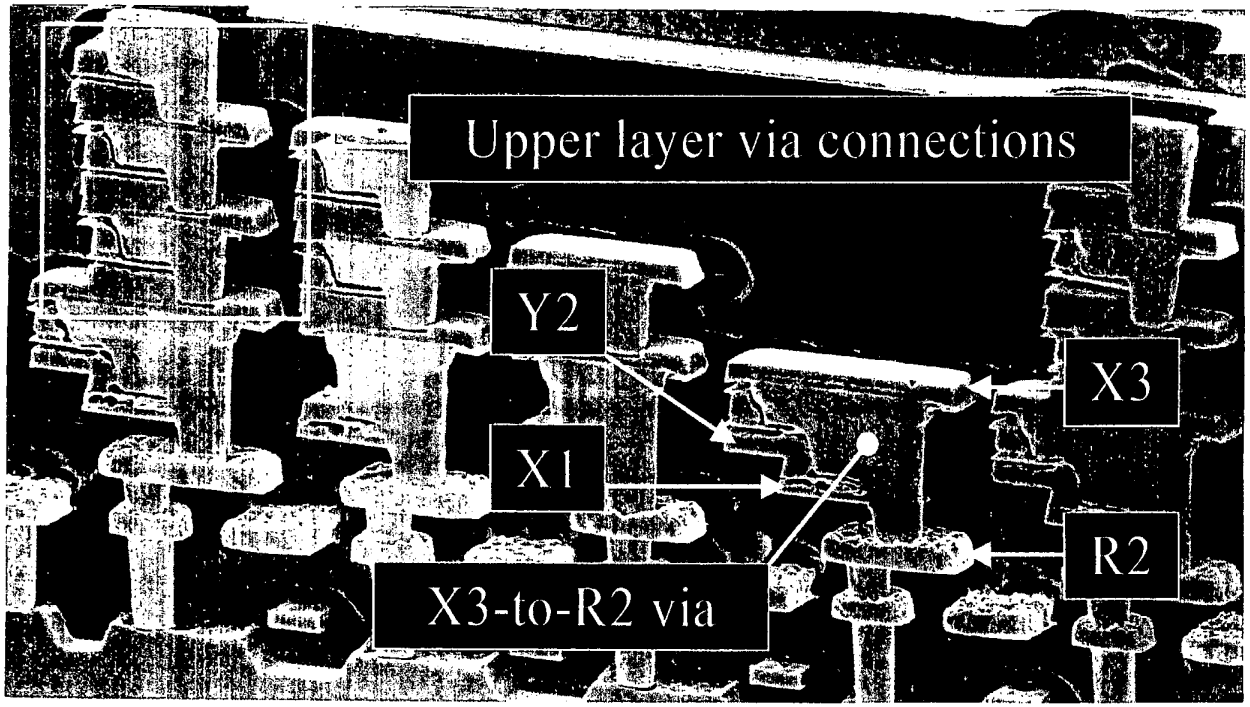


Fig. 6

New Sheet

Connections to the Array



- Vertical interconnects span 3 memory layers; 4 via masks service 9 layers.

Fig. 7

New Sheet

Tile Organization

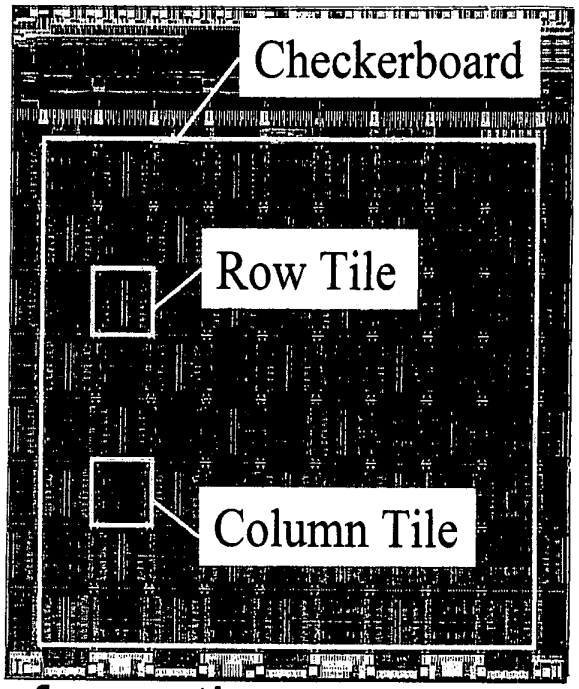
- Cells built in 1MB sub-arrays ("Tiles"):
  - 1024 wordlines x 1024 bitlines x 8 layers;
  - Additional wordlines and bitlines for test and repair.
- Row and column decoders, bias circuits, and sense amplifiers laid out beneath the 1MB Tiles.
- $2+\varepsilon$ transistors per memory line, where ε is the amortized cost of the decoders and bias circuits.

Fig. 8

New Sheet

Die Organization (1/3)

- 1MB Tiles organized in a "Checkerboard" pattern.
- Checkerboard design maximizes row and column decoder sharing.



- 1MB Tile size chosen for optimum power / BW / programmability / density.

Fig. 9

New Sheet

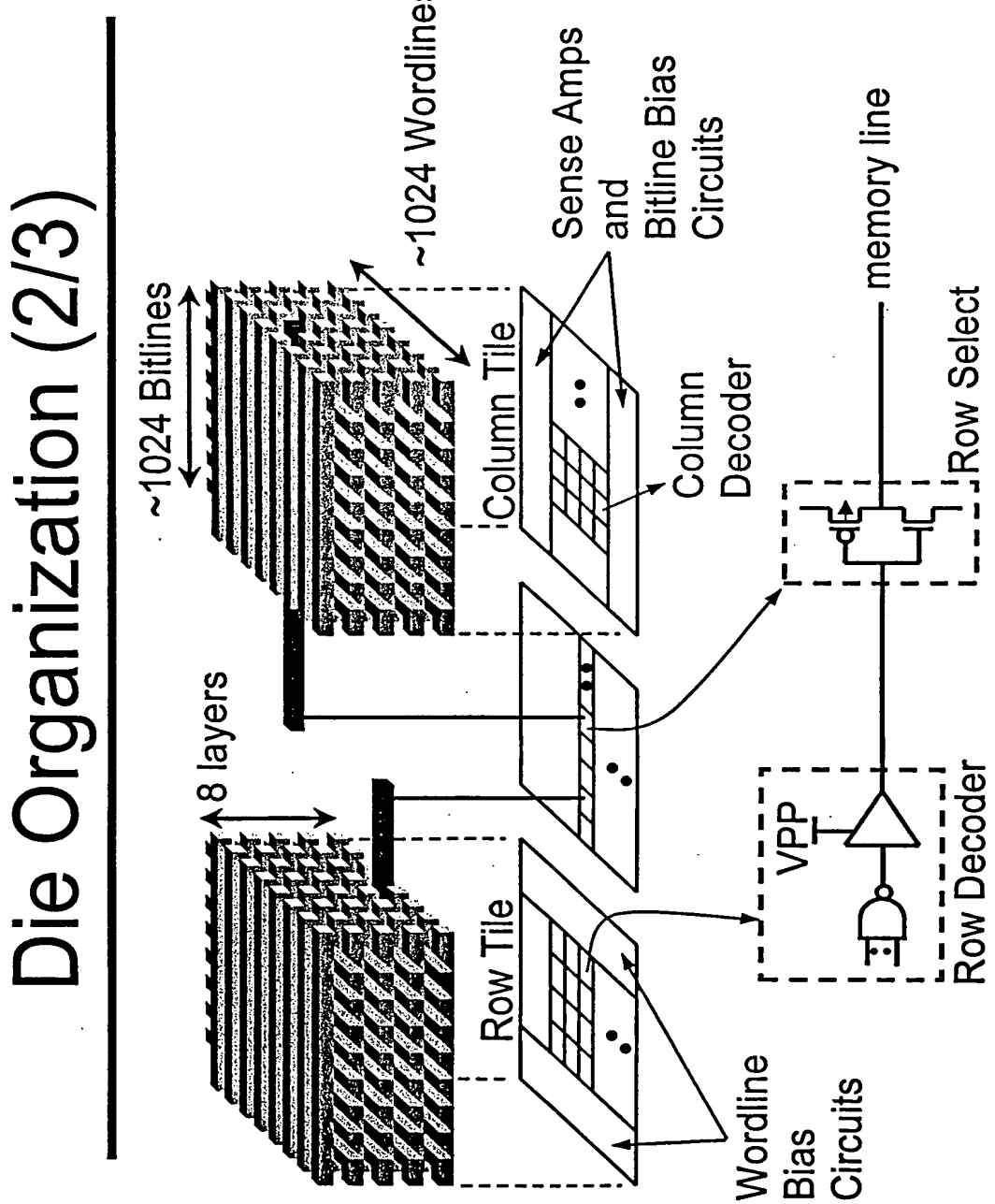

Die Organization (2/3)
~1024 Bitlines
~1024 Wordlines
8 layers
Column Tile
Sense Amps
and
Bitline Bias
Circuits
Column
Decoder
memory line
Row Select
Row Tile
VPP
Row Decoder
Wordline
Bias
Circuits

Fig. 10

Die Organization (3/3)

- Chip contains 8 horizontal Stripes, with 9 Tiles/Stripe.
- User pages are distributed among 8 Tiles in a Stripe.
- 9th Tile in each Stripe is dedicated to ECC.

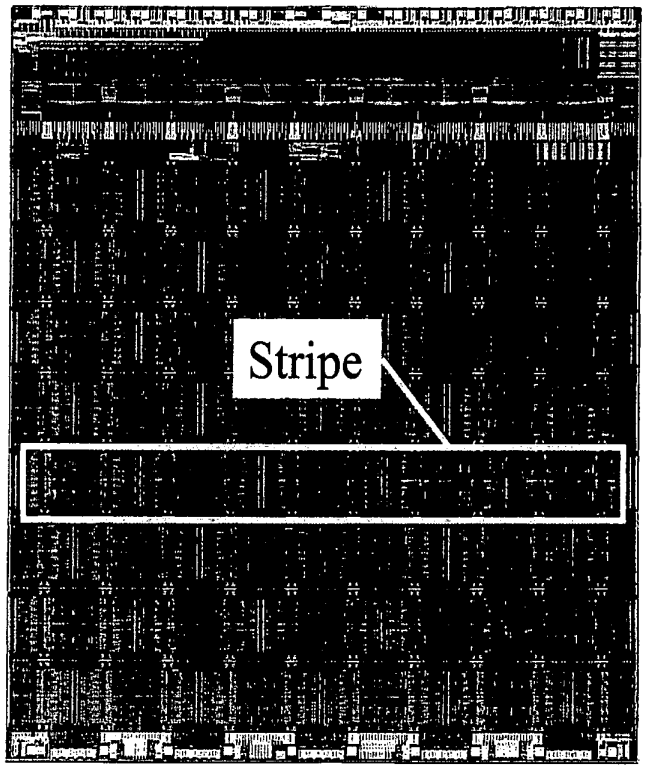


Fig. 11

New Sheet

Fault Tolerance

- Single-bit correction, double-bit detection ECC included on the die:
  - (72,64) Hamming code protection on each 64-bit "octbyte";
  - 8 additional syndrome bits per 64 user bits;
  - ECC is performed 100% on-chip; external system is unaware of ECC operations.
- Flexible row repair allows factory or on-the-fly (field) replacement.

Fig. 12

New Sheet

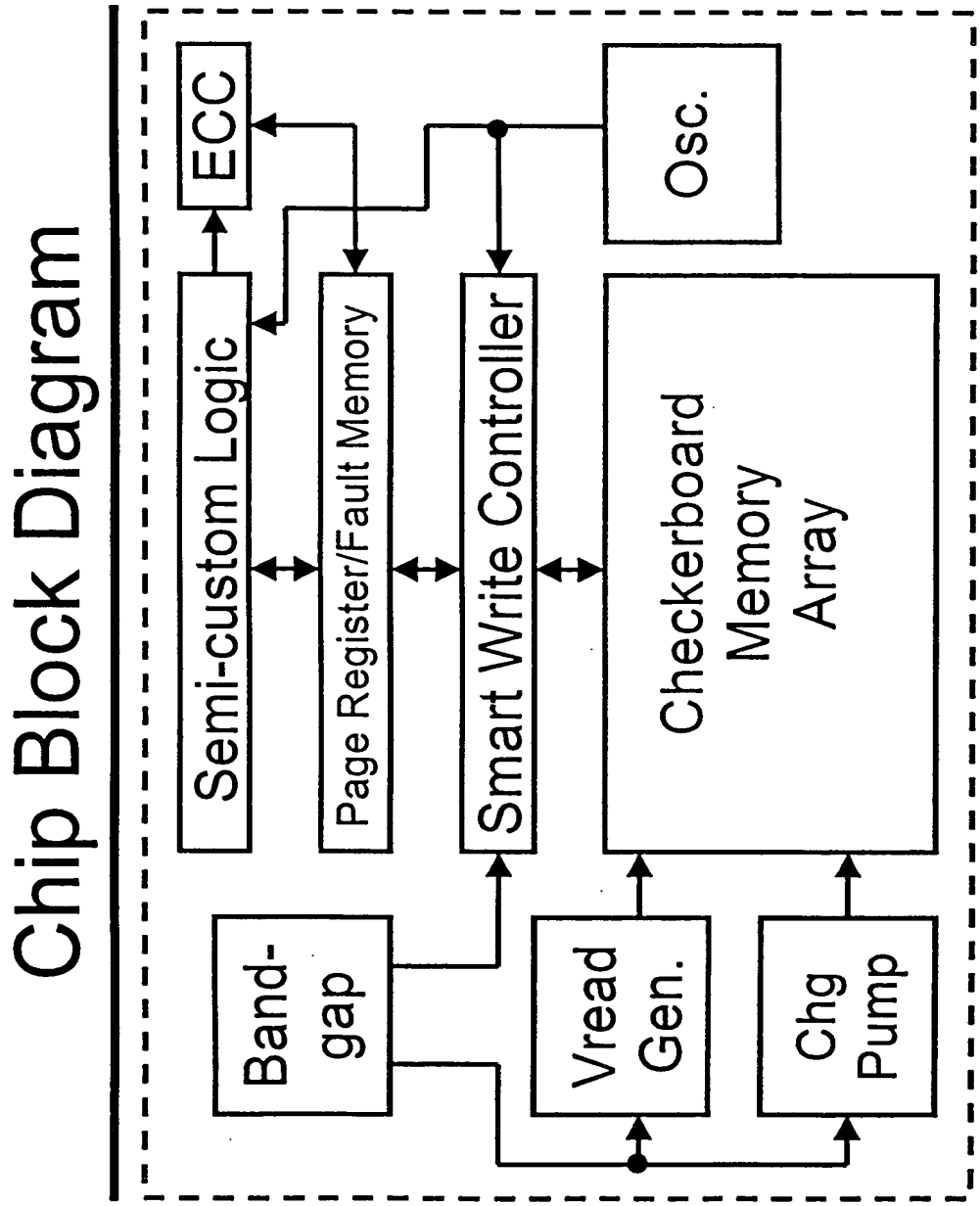

Chip Block Diagram
ECC
Semi-custom Logic
Page Register/Fault Memory
Smart Write Controller
Osc.
Checkerboard Memory Array
Band-gap
Vread Gen.
Chg Pump

Fig. 13

Write Operation (1/2)

- Write: Wordline=9V, Bitline=0V.

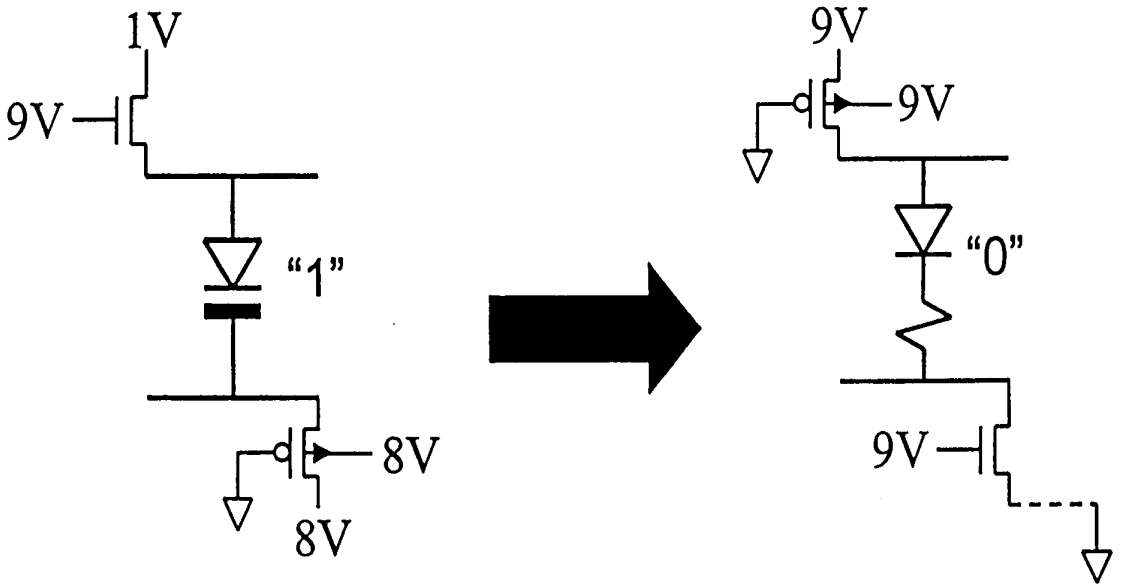


Fig. 14

New Sheet

Write Operation (2/2)

- Smart Write block:
  - Skips over "1" bits;
  - Uses the read sense amp to dynamically detect when an antifuse ruptures;
  - Immediately proceeds to the next bit, accelerating writes.
  - Detects programming fails.
- More than one fail in an ECC word (8B data + 1B ECC) initiates reprogramming to a redundant page location.

Fig. 15

New Sheet

Read Operation

- Wordline = 2.4V = "Vread".
- Bitline = Dummy bitline = 0.4V:
  - Dummy bitline provides common mode cancellation of array noise.
- Current-mode sensing:
  - Active mirror clamps memory cell voltage to 2.0V, cell current is compared to IREF.
- 72 sense amps active simultaneously:
  - All 9 Tiles in a Stripe are active;
  - Memory cells above Row Tiles are read with sense amps located in adjacent Stripes.

Fig. 16

New Sheet

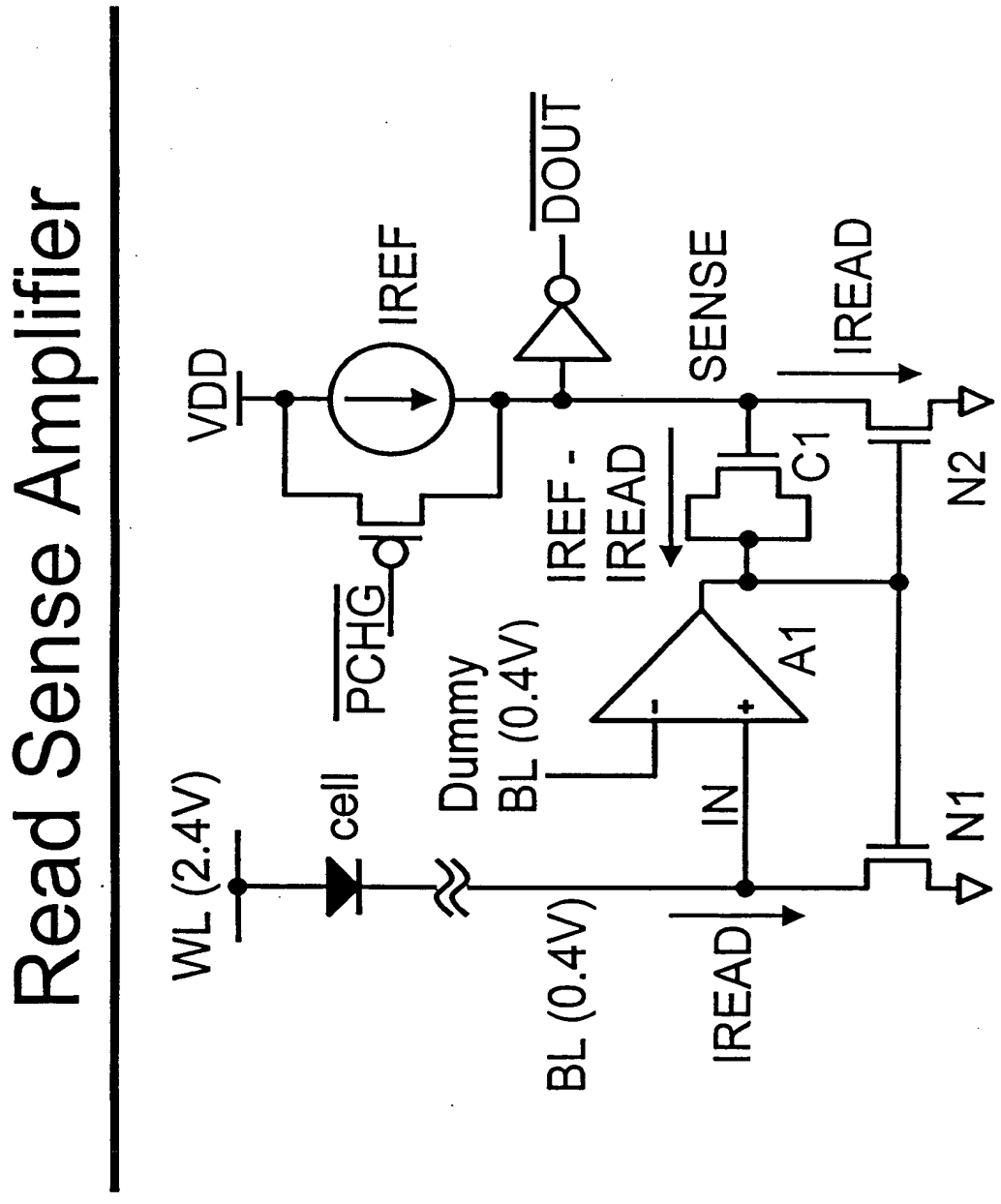

Read Sense Amplifier
WL (2.4V)
cell
PCHG
Dummy
BL (0.4V)
BL (0.4V)
VDD
IREF
IREF -
IREAD
IN
IREAD
A1
C1
SENSE
DOUT
IREAD
N2
N1

Fig. 17

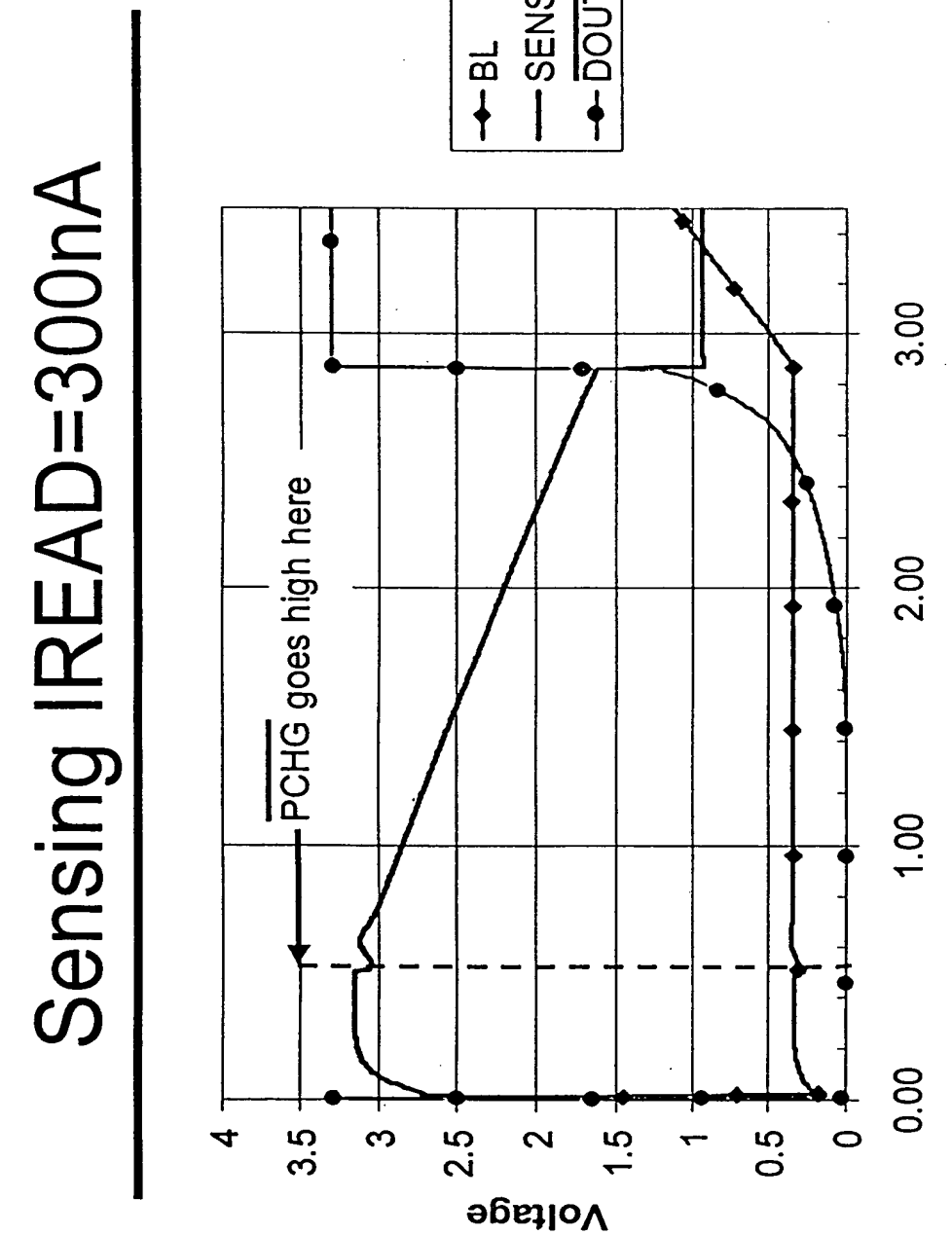

Sensing IREAD=300nA
BL
SENSE
DOUT
PCHG goes high here
Voltage
Time (microseconds)
0
0.5
1
1.5
2
2.5
3
3.5
4
0.00
1.00
2.00
3.00

Fig. 18

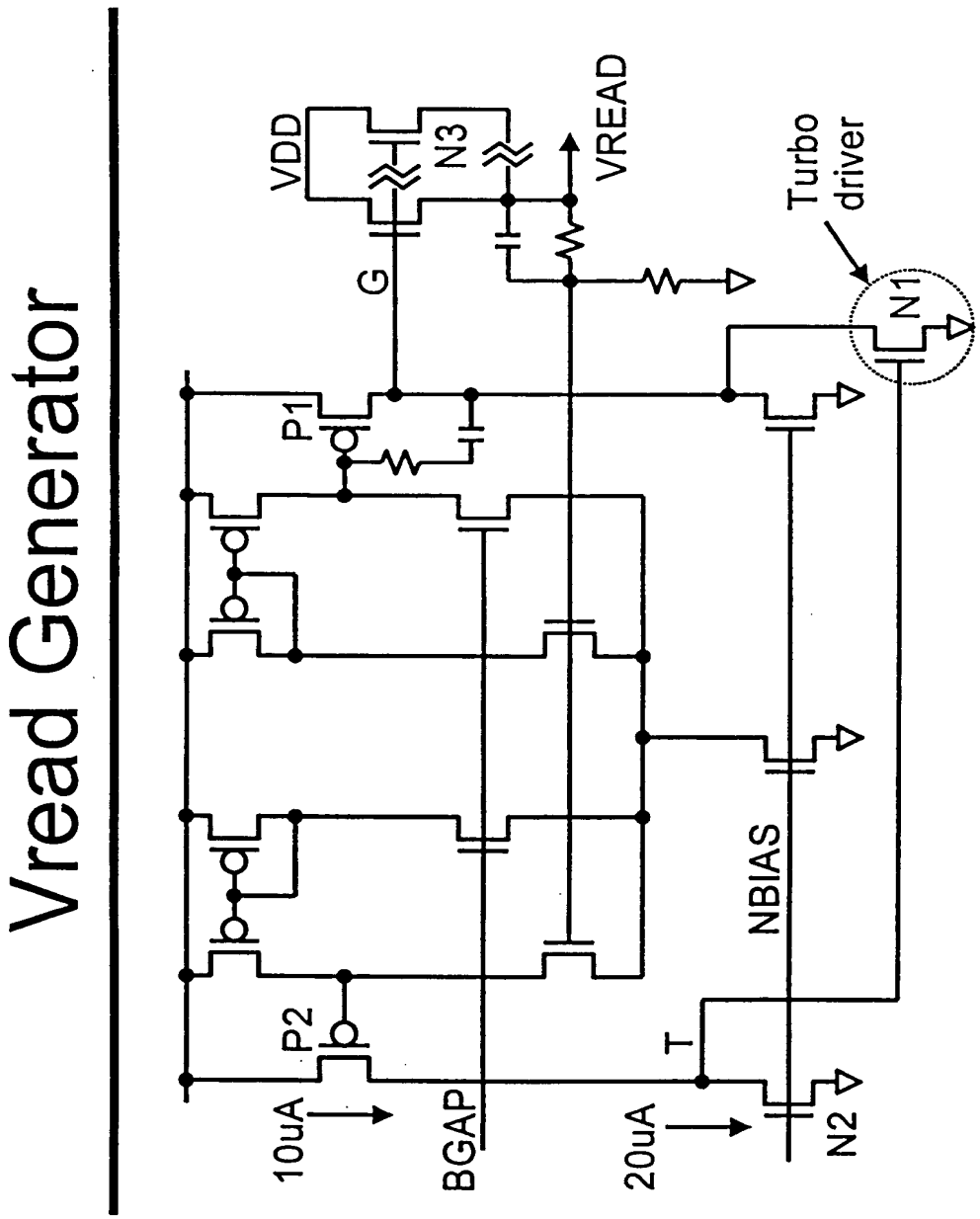

Vread Generator
VDD
N3
VREAD
G
Turbo
driver
N1
P1
P2
10uA
BGAP
20uA
T
NBIAS
N2

Fig. 19

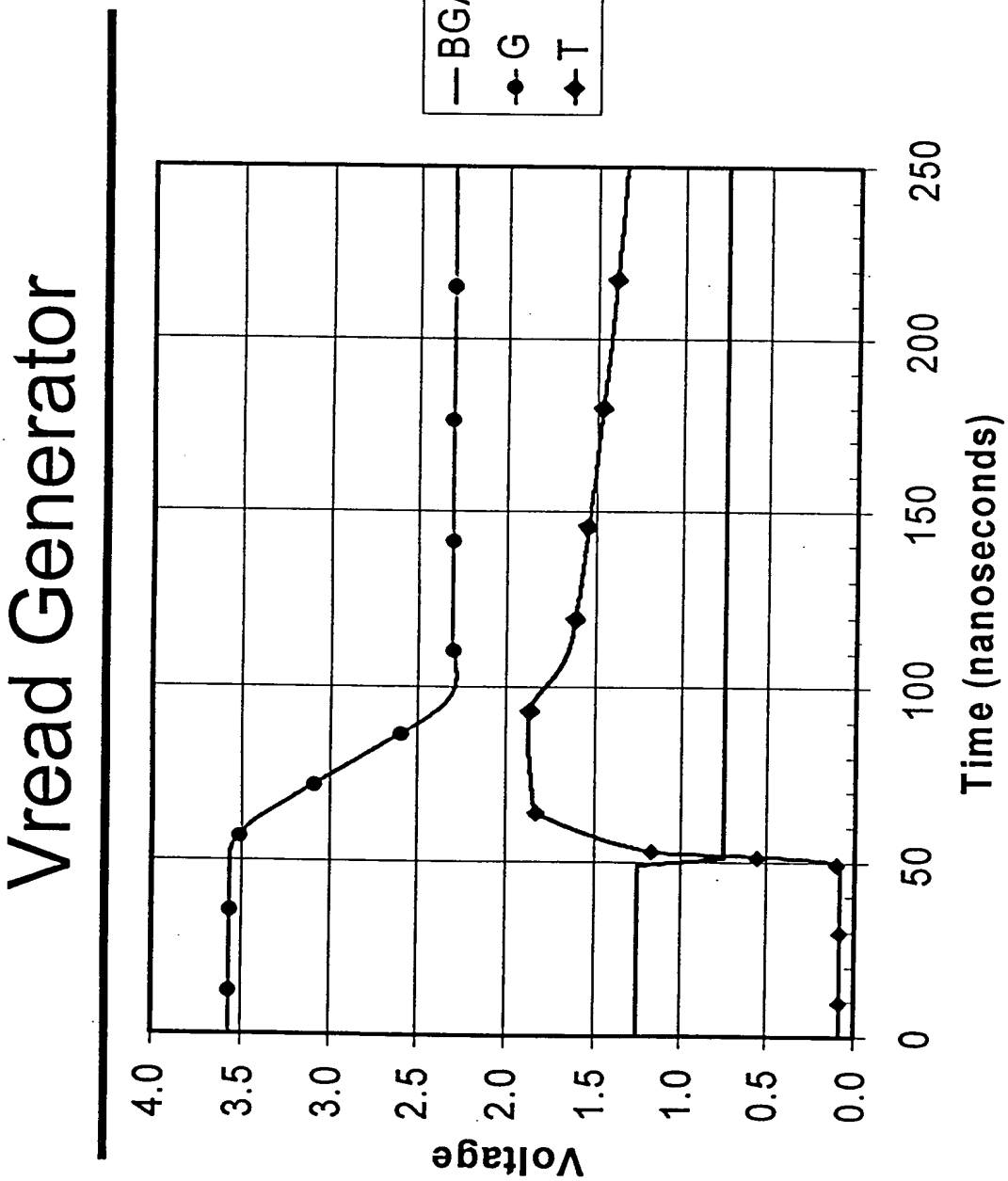

Vread Generator
BGAP
G
T
Voltage
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0
50
100
150
200
250
Time (nanoseconds)

Fig. 20

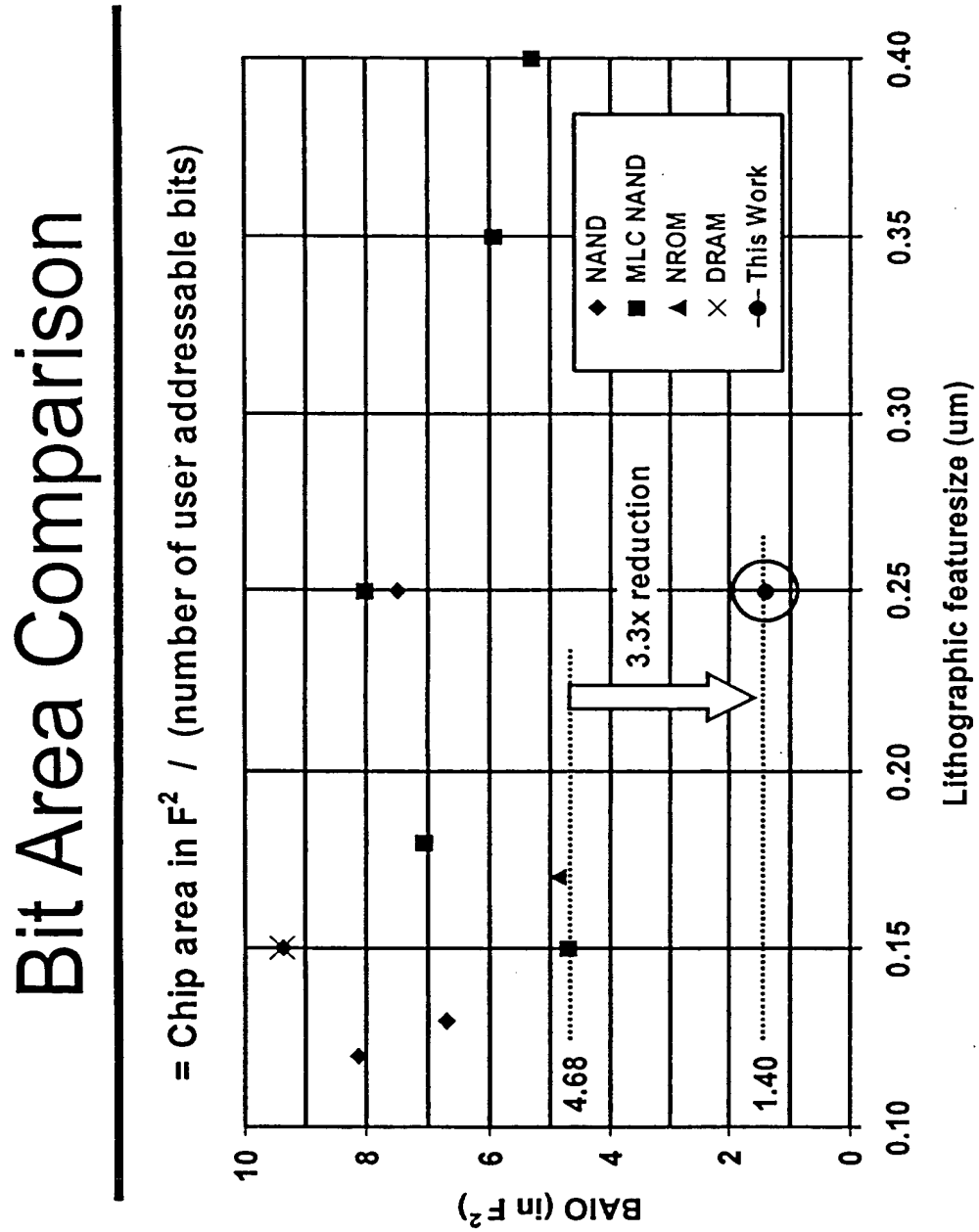

Bit Area Comparison
= Chip area in F² / (number of user addressable bits)
BAIO (in F²)
10
8
6
4
2
0
0.10
0.15
0.20
0.25
0.30
0.35
0.40
Lithographic featuresize (um)
NAND
MLC NAND
NROM
DRAM
This Work
3.3x reduction
4.68
1.40

Fig. 21

Device Characteristics

Technology	0.25um CMOS, Tox = 17.5nm
Cell type	OTP, diode+antifuse, 0 transistors
Cell size	0.50um X 0.50um
Chip size	6.7mm X 7.2mm = 48.3mm^2
Wiring	2 layers W + 1 layer Al
Power	VDD = 2.7 – 3.6V IDD = 30mA
Bandwidth	1.0 MB/s read, 0.5 MB/s write
Organization	128K pages X (512 + 16) bytes/page
Fault tolerance	(72,64) modified Hamming ECC
Application	Digital media, handhelds, file storage

Fig. 22

New Sheet

Summary

- 3-dimensional memory array with cells vertically stacked 8-high.
- Two terminal, antifuse/diode memory cell built in polysilicon.
- 512 Mbit PROM, generic NAND Flash interface.
- SEC-DED ECC included on-die.
- 3.3x more bits per F^2 than MLC NAND Flash.

Fig. 23

New Sheet